CLAIMS

What is claimed is:

1. A capacitor comprising:

m electrode plates;

wherein each of said m electrode plates are arranged spaced apart in parallel;

wherein m is an integer greater than 1;

wherein each of said m electrode plates comprises a first extension;

n first external terminals;

wherein n is an integer greater than 1;

wherein said n first external terminals are arranged on a first common exterior surface of the capacitor;

wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals;

wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals;

wherein said n first external terminals are arranged at a predefined minimal distance from each other to minimize parasitic inductance.

2. The capacitor of claim 1, wherein said predefined minimal distance is a minimal distance that prevents crosstalk between said n first external terminals.

3. The capacitor of claim 1, wherein said n first external terminals are arranged in parallel.

4. The capacitor of claim 1, wherein n=2; wherein said n first external terminals are arranged in parallel.

5. The capacitor of claim 1, wherein n=3; wherein said n first external terminals are arranged in parallel and wherein said even one of said n first external terminals is arranged between the odd ones of said n first external terminals.

6. The capacitor of claim 1, wherein a dielectric material is disposed between each of said m electrode plates.

7. The capacitor of claim 6, wherein said dielectric material is ceramic material.

8. The capacitor of claim 1, wherein exterior ones of said n first external terminals are disposed on said common exterior surface of said capacitor and corresponding side surfaces of said capacitor.

9. The capacitor of Claim 1, wherein n is 4;

wherein a first one and a second one of said n first external terminals are arranged in a first row;

wherein a third one and a fourth one of said n first external terminals are arranged in a second row;

wherein said first one of said n first external terminals is arranged adjacent said second and fourth ones of said n first external terminals and diagonal to said third one of said n first external terminals;

wherein said second one of said n first external terminals is arranged diagonal to said fourth one of said n first external terminals.

10. The capacitor of Claim 1,

wherein each of said m electrode plates comprises a second extension;

wherein said capacitor comprises s second external terminals;

wherein s is an integer greater than 1;

wherein said s second external terminals are arranged on a second common exterior surface of the capacitor;

wherein said second extensions of said even ones of said m electrode plates are coupled to said even ones of said s second external terminals;

wherein said second extensions of said odd ones of said m electrode plates are coupled to odd ones of said s second external terminals.

11. The capacitor of Claim 10, wherein said second common exterior surface is arranged opposite to said first common exterior surface.

12. The capacitor of Claim 1,

wherein each of said m electrodes comprises a second extension;

wherein the capacitor comprises s second external terminals;

wherein s is an integer greater than 1;

wherein even ones of said s second external terminals are arranged on a third exterior surface of the capacitor;

wherein odd ones of said s second external terminals are arranged on a fourth exterior surface of the capacitor;

wherein said second extensions of even ones of said m electrode plates are coupled to even ones of said s second external terminals; and

wherein said second extensions of odd ones of said m electrode plates are coupled to odd ones of said s second external terminals.

13. The capacitor of Claim 12, wherein said third exterior surface is arranged opposite to said fourth exterior surface.

14. The capacitor of claim 1, further comprising a housing that encloses at least a part of said capacitor.

15. The capacitor of claim 1, wherein height of said capacitor is greater than width of said capacitor.

16. The capacitor of claim 1, wherein a portion of at least one of said n first external terminals wraps around a corner of said capacitor.

17. The capacitor of claim 1,wherein said n first external terminals have a bar structure.

18. A filter comprising:

an inductor;

a capacitor of Claim 1,

wherein said inductor is connected to even ones of said n first external terminals;

wherein an output terminal is connected to even ones of said n first external terminals; and

wherein a reference voltage is connected to odd ones of said n first external terminals.

19. The filter of claim 18,

wherein n=3;

wherein said n first external terminals are arranged in parallel and wherein said even one of said n first external terminals is arranged between the odd ones of said n first external terminals;

wherein first and third ones of said n first external terminals are coupled to the reference voltage;

wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals; and

wherein the output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

20. The filter of claim 18,

wherein n=2;

wherein said n first external terminals are arranged in parallel;

wherein first one of said n first external terminals is coupled to a reference voltage ;

wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals; and

wherein an output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

21. A voltage regulator comprising the filter of claim 18.

22. The voltage regulator of claim 21 further comprising a multilayer printed circuit board;

wherein said capacitor is mounted on said multilayer printed circuit board;

wherein said inductor is connected to a first trace of said multilayer printed circuit board;

wherein said first trace is connected to said even ones of said n first external terminals by way of a first plurality of vias;

wherein said output terminal is connected to a second trace on said multilayer printed circuit board;

wherein said second trace is connected to said even ones of said n first external terminals by way of a second plurality of vias;

wherein the reference voltage is connected to a third trace on said multilayer printed circuit board; and

wherein said third trace is connected to said odd ones of said n first external terminals by way of a third plurality of vias.

23. A printed circuit board ("PCB") comprising:

a plurality of PCB contacts; and

a plurality of capacitors of Claim 1 coupled to said plurality of PCB contacts to facilitate parallel connections of at least two capacitors.

24. A capacitor structure comprising:

a first capacitor comprising:

m electrode plates;

wherein each of said m electrode plates are arranged spaced apart in parallel;

wherein m is an integer greater than 1;

wherein each of said m electrodes comprises a first extension;

wherein each of said m electrodes comprises a second extension;

n first external terminals;

wherein n is an integer greater than 1;

wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor;

wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals;

wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals;

s second external terminals;

wherein s is an integer greater than 1;

wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor;

wherein said second extension of even ones of said m electrode plates are coupled to even ones of said s second external terminals;

wherein said second extension of odd ones of said m electrode plates are coupled to odd ones of said s second external terminals

a second capacitor comprising:

x electrode plates;

wherein each of said x electrode plates are arranged in parallel;

wherein x is an integer greater than 1;

wherein each of said x electrodes comprises a third extension;

s third external terminals;

wherein said s third external terminals are arranged on a third common exterior surface of said second capacitor;

wherein said third extension of even ones of said x electrode plates are coupled to even ones of said s third external terminals;

wherein said third extension of odd ones of said x electrode plates are coupled to odd ones of said s third external terminals;

wherein said second capacitor is mounted on said first capacitor; and

wherein said s third external terminals are coupled to corresponding ones of said s second external terminals.

25. The capacitor structure of claim 24, further comprising a housing that encloses at least a part of said first and said second capacitors.

26. The capacitor structure of claim 24, wherein said n first external terminals are arranged in parallel; wherein said s second external terminals are arranged in parallel; and wherein said s third external terminals are arranged in parallel.

27. The capacitor structure of claim 24, wherein s=2; wherein said s second external terminals are arranged in parallel and wherein said s third external terminals are arranged in parallel.

28. The capacitor structure of claim 24, wherein s=3; wherein said s second external terminals are arranged in parallel and wherein said even one of said s second external terminals is arranged between the odd ones of said s second external terminals and wherein said s third external terminals are arranged in parallel and wherein said even one of said s third external terminals is arranged between the odd ones of said s third external terminals.

29. The capacitor structure of claim 24, wherein a first dielectric material is disposed between each of said m electrode plates of said first capacitor; and wherein a second dielectric material is disposed between each of said x electrode plates of said second capacitor.

30. The capacitor structure of 29, wherein said first and second dielectric material are different.

31. The capacitor structure of 29, wherein said first and second dielectric material are the same.

32. The capacitor structure of claim 29, wherein at least one of said first dielectric material and said second dielectric material comprises a ceramic material.

33. The capacitor structure of Claim 24, wherein s is 4;

wherein a first one and a second one of said s second external terminals are arranged in a first row;

wherein a third one and a fourth one of said s second external terminals are arranged in a second row;

wherein said first one of said s second external terminals is arranged adjacent to said second and fourth ones of said s second external terminals and diagonal to said third one of said s second external terminals;

wherein said second one of said s second external terminals is arranged diagonal to said fourth one of said s second external terminals;

wherein a first one and a second one of said s third external terminals are arranged in a first row;

wherein a third one and a fourth one of said s third external terminals are arranged in a second row;

wherein said first one of said s third external terminals is arranged adjacent to said second and fourth ones of said s third external terminals and diagonal to said third one of said s third external terminals; and

wherein said second one of said s third external terminals is arranged diagonal to said fourth one of said s third external terminals.

34. The capacitor structure of Claim 24,

wherein each of said x electrodes plates comprises a fourth extension;

wherein said capacitor comprises u fourth external terminals;

wherein u is an integer greater than 1;

wherein said u fourth external terminals are arranged on a fourth common exterior surface of said second capacitor;

wherein said fourth extensions of said even ones of said x electrode plates are coupled to said even ones of said u fourth external terminals;

wherein said fourth extensions of said odd ones of said x electrode plates are coupled to odd ones of said u fourth external terminals.

35. The capacitor structure of Claim 34, wherein said third common exterior surface is arranged opposite to said fourth common exterior surface.

36. The capacitor structure of claim 24,wherein said s second and s third external terminals have a bar structure.

37. A filter comprising:

an inductor;

a capacitor structure of Claim 24;

wherein said inductor is connected to even ones of said n first external terminals;

wherein an output terminal is connected to even ones of said n first external terminals; and

wherein a reference voltage is connected to odd ones of said n first external terminals.

38. The filter of claim 37, wherein n=3;

wherein said n first external terminals are arranged in parallel and wherein said even one of said n first external terminals is arranged between the odd ones of said n first external terminals;

wherein first and third ones of said n first external terminals are coupled to the reference voltage;

wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals; and

wherein the output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

39. The filter of claim 37, wherein n=2;

wherein said n first external terminals are arranged in parallel;

wherein first one of said n first external terminals is coupled to a reference voltage;

wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals; and

wherein an output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

40. A voltage regulator comprising the filter of claim 37 further comprising a multilayer printed circuit board; wherein said capacitor structure is mounted on said multilayer printed circuit board;

wherein said inductor is connected to a first trace of said multilayer printed circuit board; and

wherein said first trace is connected to said even ones of said n first external terminals by way of a first plurality of vias;

wherein said output terminal is connected to a second trace on said multilayer printed circuit board;

wherein said second trace is connected to said even ones of said n first external terminals by way of a second plurality of vias;

wherein the reference voltage is connected to a third trace on said multilayer printed circuit board; and

wherein said third trace is connected to said odd ones of said n first external terminals by way of a third plurality of vias.

41. A capacitor structure comprising:

a first capacitor comprising:

m electrode plates;

wherein each of said m electrode plates are arranged spaced apart in parallel;

wherein m is an integer greater than 1;

wherein each of said m electrodes comprises a first extension and a second extension;

n first external terminals;

wherein n is an integer greater than 1;

wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor;

wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals;

wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals;;

s second external terminals;

wherein s is an integer greater than 0;

wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor;

wherein said second extension of even ones of said m electrode plates are coupled to said s second external terminals;

a second capacitor comprising:

x electrode plates;

wherein each of said x electrode plates are arranged spaced apart in parallel;

wherein x is an integer greater than 1;

wherein each of said x electrodes comprises a third extension;

s third external terminals;

wherein said s third external terminals are arranged on a third common exterior surface of said second capacitor;

wherein said third extension of even ones of said x electrode plates are coupled to said s third external terminals;

wherein said second capacitor is disposed adjacent to said first capacitor;

wherein said s third external terminals are coupled to corresponding ones of said s second terminals.

42. The capacitor structure of claim 41, wherein said n first external terminals are arranged in parallel; wherein said s second external terminals are arranged in parallel; and wherein said s third external terminals are arranged in parallel.

43. The capacitor structure of claim 41, wherein s=2; wherein said s second external terminals are arranged in parallel and wherein said s third external terminals are arranged in parallel.

44. The capacitor structure of claim 41, wherein s=3; wherein said s second external terminals are arranged in parallel and wherein said even one of said s second external terminals is arranged between the odd ones of said n second external terminals and wherein said s third external terminals are arranged in parallel and wherein said even one of said s third external terminals is arranged between the odd ones of said s third external terminals.

45. The capacitor structure of claim 41, wherein a first dielectric material is disposed between each of said m electrode plates of said first capacitor; and wherein a second dielectric material is disposed between each of said x electrode plates of said second capacitor.

46. The capacitor structure of 45, wherein said first and second dielectric material are different.

47. The capacitor structure of 45, wherein said first and second dielectric material are the same.

48. The capacitor of claim 41, wherein said n first external terminals are arranged in parallel.

49. The capacitor of claim 41, wherein n=2; wherein said n first external terminals are arranged in parallel.

50. The capacitor of claim 41, wherein n=3; wherein said n first external terminals are arranged in parallel and wherein said even one of said n first external terminals is arranged between the odd ones of said n first external terminals.

51. The capacitor of claim 45, wherein at least one of said first second dielectric material and said second dielectric material comprises a ceramic material.

52. The capacitor of Claim 41, wherein n is 4;

wherein a first one and a second one of said n first external terminals are arranged in a first row;

wherein a third one and a fourth one of said n first external terminals are arranged in a second row;

wherein said first one of said n first external terminals is arranged adjacent to said second and fourth ones of said n first external terminals and diagonal to said third one of said n first external terminals; and

wherein said second one of said n first external terminals is arranged diagonal to said fourth one of said n first external terminals.

53. The capacitor of claim 41,wherein said n first external terminals have a bar structure.

54. A filter comprising:

an inductor;

a capacitor of Claim 41;

wherein said inductor is connected to even ones of said n first external terminals;

wherein an output terminal is connected to even ones of said n first external terminals; and

wherein a reference voltage is connected to odd ones of said n first external terminals.

55. The filter of claim 54, wherein n=3;

wherein said n first external terminals are arranged in parallel and wherein said even one of said n first external terminals is arranged between the odd ones of said n first external terminals;

wherein first and third ones of said n first external terminals are coupled to the reference voltage;

wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals; and

wherein the output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

56. The filter of claim 54, wherein n=2;

wherein said n first external terminals are arranged in parallel;

wherein first one of said n first external terminals is coupled to a reference voltage;

wherein one terminal of said inductor is coupled to a first end portion of a second one of said n first external terminals; and

wherein an output terminal of said filter is provided at a second end portion of said second one of said n first external terminals.

57. A voltage regulator comprising the filter of claim 54 further comprising a multilayer printed circuit board; wherein said capacitor structure is mounted on said multilayer printed circuit board;

wherein said inductor is connected to a first trace of said multilayer printed circuit board; and

wherein said first trace is connected to said even ones of said n first external terminals by way of a first plurality of vias;

wherein said output terminal is connected to a second trace on said multilayer printed circuit board;

wherein said second trace is connected to said even ones of said n first external terminals by way of a second plurality of vias;

wherein the reference voltage is connected to a third trace on said multilayer printed circuit board; and

wherein said third trace is connected to said odd ones of said n first external terminals by way of a third plurality of vias.

58. The filter of claim 54, wherein s=1;

wherein said s second external terminal is coupled to even ones of said m electrode plates; and

wherein said s third external terminal is coupled to even ones of said x electrode plates.

59. The capacitor structure of claim 41, wherein at least one of said s second external terminals extend from said second common exterior surface to said first common exterior surface of said first capacitor by wrapping around a corner of said first capacitor.

60. A printed circuit board ("PCB") comprising:

a plurality of PCB contacts; and

a plurality of capacitor structures of Claim 41 coupled to said plurality of PCB contacts to provide parallel connections of at least two capacitors.

61. A device comprising:

a first capacitor comprising;

m electrode plates;

wherein each of said m electrode plates are arranged spaced apart in parallel;

wherein m is an integer greater than 1;

wherein each of said m electrodes comprises a first extension;

wherein w electrode plates of said m electrode plates comprise a second extension, wherein w is an integer less than m;

n first external terminals;

wherein n is an integer greater than 1;

wherein said n first external terminals are arranged on a first common exterior surface of said first capacitor;

wherein said first extension of even ones of said m electrode plates are coupled to even ones of said n first external terminals;

wherein said first extension of odd ones of said m electrode plates are coupled to odd ones of said n first external terminals;

s second external terminals;

wherein s is an integer greater than 1;

wherein said s second external terminals are arranged on a second common exterior surface of the first capacitor;

wherein said second extension of even ones of said w electrode plates are coupled to even ones of said s second external terminals;

wherein said second extension of odd ones of said w electrode plates are coupled to odd ones of said s second external terminals;

a second capacitor comprising:

x electrode plates;

wherein each of said x electrode plates are arranged spaced apart in parallel;

wherein x is an integer greater than 1;

wherein y electrode plates of said x electrode plates comprise a third extension;

wherein y is an integer less than x;

q third external terminals;

wherein q is an integer greater than 1;

wherein said q third external terminals are arranged on a third common exterior surface of said second capacitor;

wherein said third extension of even ones of said y electrode plates are coupled to even ones of said q third external terminals;

wherein said third extension of odd ones of said y electrode plates are coupled to odd ones of said q third external terminals;

wherein said second capacitor is disposed abutting and adjacent to said first capacitor;

wherein said even ones of said q third external terminals are coupled to said even ones of said s second terminals; and

wherein said odd ones of said q third external terminals are coupled to said odd ones of said s second terminals.

62. The device of claim 61,

wherein z electrode plates of said m electrode plates comprise a fourth extension ;

wherein sum of y and z is integer less than or equal to m;

wherein the first capacitor further comprises f fourth external terminals;

wherein f is an integer greater than 1;

wherein said f fourth external terminals are arranged on a fourth common exterior surface of said first capacitor; wherein said fourth common exterior surface is opposite to said second common exterior surface;

wherein said fourth extension of even ones of said z electrode plates are coupled to even ones of said f fourth external terminals; and

wherein said third extension of odd ones of said z electrode plates are coupled to odd ones of said f fourth external terminals.

63. A circuit comprising:

a printed circuit board ("PCB") including a plurality of PCB contacts longitudinally arranged in parallel; and

a plurality of capacitors wherein each of said capacitors is arranged abutting with each other and mounted on said PCB; wherein each of said plurality of capacitors comprises said capacitor of Claim 1.

64. The capacitor of Claim 10, wherein said second common exterior surface is arranged substantially orthogonal to said first common exterior surface. .

65. The capacitor of Claim 12, wherein said third and fourth common exterior surfaces are arranged substantially orthogonal to said first common exterior surface. .

66. The capacitor of Claim 1,

wherein each of said m electrodes comprises a second extension;

wherein the capacitor comprises s second external terminals;

wherein s is an integer greater than 1;

wherein even ones of said s second external terminals are arranged on a third exterior surface of the capacitor;

wherein odd ones of said s second external terminals are arranged on a third exterior surface of the capacitor;

wherein said second extensions of even ones of said m electrode plates are coupled to even ones of said s second external terminals; and

wherein said second extensions of odd ones of said m electrode plates are coupled to odd ones of said s second external terminals.

66. The capacitor of Claim 66, wherein said odd ones of said s second external terminals are arranged space apart and parallel to said even ones of said s second external terminals. .

67. The capacitor of claim 14, wherein said housing is formed from an ejection molding process.

68. The capacitor of claim 1, further comprising an encapsulation that encloses at least a part of said capacitor.

69. The capacitor of Claim 24, wherein said second common exterior surface is arranged substantially orthogonal to said first common exterior surface. .

70. The capacitor structure of claim 25, wherein said housing is formed from an ejection molding process.

71. The capacitor structure of claim 24, further comprising an encapsulation that encloses at least a part of said first and second capacitors.

72. The capacitor structure of Claim 24,

wherein each of said x electrodes plates comprises a fourth extension;

wherein said capacitor comprises u fourth external terminals;

wherein u is an integer greater than 1;

wherein said u fourth external terminals are arranged on said third common exterior surface of said second capacitor;

wherein said fourth extensions of said even ones of said x electrode plates are coupled to said even ones of said u fourth external terminals;

wherein said fourth extensions of said odd ones of said x electrode plates are coupled to odd ones of said u fourth external terminals.

73. The capacitor structure of Claim 41, wherein said second common exterior surface is arranged substantially orthogonal to said first common exterior surface,

wherein said third common exterior surface is arranged substantially orthogonal to said fourth common exterior surface. .

74. The device of claim 61, further comprising a housing that encloses at least a part of said device. .

75. The device of claim 74, wherein said housing is formed from an ejection molding process.

76. The device of claim 61, further comprising an encapsulation that encloses at least a part of said device.

77. The device of claim 1, wherein the predefined minimal distance is less than 12 mils.

78. The device of claim 1, wherein the predefined minimal distance is less than 8 mils.

79. The capacitor structure of claim 25, wherein the housing comprises a fin to dissipate heat from said first and second capacitors..